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10/743,218	12/22/2003	Timothy J. Dupuis	SIL.P0069	7652

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EXAMINER	
NGUYEN, DUC M	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,218	DUPUIS, TIMOTHY J.	
	Examiner	Art Unit	
	Duc M. Nguyen	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/29/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to applicant's response filed on 6/18/07. Claims 1, 3-47 are now pending in the present application.

Information Disclosure Statement

2. The references listed in the information disclosure statements submitted on 6/29/07 has been considered by the examiner (see attached PTO-1449).

Response to Arguments

3. Applicant's arguments filed 6/18/07 have been fully considered but they are not persuasive.

In the response filed 6/18/07, Applicant contends that

> Bell discloses an amplifier circuit using an automatic gain control (AGC). The circuit of Bell is designed to adjust the gain of amplifier 14 so that the output Vout is maintained at a desired RMS value. Bell uses an analog reference voltage Vref to maintain the RMS value of Vout. Blake discloses an programmable gain amplifier. Blake discloses an external analog reference voltage Vref that is connected to a gain setting resistor ladder network 112. In both Bell and Blake, Vref is not a digital signal, but rather is an analog reference voltage. Also, it appears that Vref is constant, and therefore is not used to vary the output power of an amplifier based on a desired output power level that relates to a digital signal from an external controller. It is unclear from the Blake reference how Vref could be a digital signal from an external controller, likewise with Bell. The Office Action also states that that the logical circuits in FIGS. 6A and 6B of Bell are digital interfaces. FIGS. 6A and 6B of Bell show the gain latch, ripple counter, delay and reset control circuitry shown in FIG. 1. It is also unclear how these could be interfaces that meet the requirements of amended claim 1.

In response, the Examiner asserts that both Bell and Blake do not teach the reference voltage Vref is an **analog** signal, noting that Applicant has failed to provide any paragraph in Bell's or Blake's references that would support his/her allegation. In fact, the logical circuits in FIGS. 6A and 6B of Bell are digital circuits and would read on the digital interfaces as claimed, noting for the clock pulse and binary values in col. 4,

lines 30-51 of Bell reference, which would suggest a digital input to the ramp generator. Further, the digital signal processor in Fig. 2 of Blake's reference clearly suggests that the Vref is a digital signal. Further, one skilled in the art would recognize that the Vref is the desired output power level.

One pages 11-12, Applicant further contends that

Lee discloses a wireless local area network (WLAN) transceiving integrated circuit (IC), including a WLAN interface, an input buffer and controller, and a processor. An IC of Lee (e.g., IC 350 of FIG. 3B) includes a power amplifier 352, core components 351, and serial and parallel interfaces 320 and 324 to interface with a host 322. An IC of Lee (e.g., IC 400 of FIG. 4A) may include a baseband 404. Lee does not teach or suggest, however, an integrated circuit with a digital interface for providing an interface between the power amplifier circuitry and an external controller, wherein the interface is a digital interface for receiving a digital signal from the external controller, and wherein the digital signal contains power control data. The interface between the power amplifier 352 and the core components 351 (FIG. 3B) appears to include an transmit signal TX and an analog power control signal TX_PC. The interfaces 320 and 324 (FIG. 3B) do not provide an interface between the power amplifier 352 and an external controller.

Lin discloses a wireless transmission apparatus used for transmitting an RF signal. Like Lee, Lin also does not teach or suggest an integrated circuit with a digital interface for providing an interface between the power amplifier circuitry and an external controller, wherein the interface is a digital interface for receiving a digital signal from the extemal controller, and wherein the digital signal contains power control data. The power amplifier 118 receives an RF input signal R118 and an analog control signal from the power control loop 116.

The Office Action states that Blake discloses a digital interface for controlling a power amplifier. Applicants assert that the analog reference voltage Vref does not meet the requirements of amended claim 1, as is discussed in detail above.

In response, the Examiner asserts that **Lee** does not teach the power control signal TX_PC is an **analog** signal, noting that Applicant has failed to provide any paragraph in Lee's references that would support his/her allegation. In fact, in paragraph [0053], Lee teaches a power manage unit 447 that "provides power management features that are controlled through setting of the power management registers". This **register** feature clearly suggests digital signals for the settings, not to mention many digital serial interfaces for the wireless IC circuits disclosed through out the **Lee** reference.

Therefore, Lee would obviously teach, or be modified to provide a digital interface for controlling the power of the amplifier in the similar way as disclosed by Blake, for minimizing pin count of the amplifier IC package (see Blake, col. 5, lines 55-60).

For foregoing reasons, the examiner believes that the pending claims 1, 3-47 which rely on the patentability of an external digital control signal for controlling the power of an amplifier are not allowable over the cited prior art.

Claim Rejections - 35 USC ∋ 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **1, 3, 16** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Bell** (US 5,642,075) in view of **Blake** (US 6,847,904).

Regarding claim **1**, **Bell** discloses an RF apparatus formed using an integrated circuit (see col. 2, lines 23-37), comprising

- an amplifier circuitry formed using the integrated circuit (see Fig. 1 and col. 2, lines 23-37) and
- circuitry for generating a power ramp profile to control the output power of the RF power amplifier (see Fig. 1, wherein the ramp generator would read on the ramp profile).

Although **Bell** does not specifically disclose the amplifier is the power amplifier, one skilled in the art would recognize that an power amplifier would work equally well with Bell's teaching. Therefore, the claimed limitation regarding the power amplifier is made obvious by Bell.

As to the newly added limitation regarding a digital interface for providing an interface between the power amplifier circuit and an external controller, it is noted that the logical circuits in Figs. 6A, 6B of Bell are digital interfaces (see Figs. 6A, 6B), and that the Vref as shown in Fig. 1 of Bell for controlling the gain of the amplifier would obviously be a digital signal as an external controller for controlling the amplifier to a desired output level in the similar way as disclosed by **Blake** (see Fig. 1 and col. 6, lines 20-24). Therefore, the claimed limitation regarding the newly added limitation is made obvious by Bell, in view of Blake.

Regarding claim **3,** it is clear that the digital interface would inherently comprise serial interfaces (see also Blake, Abstract).

Regarding claim **16,** Bell discloses a digital to analog converter circuit (17) formed using the integrated circuit for generating a power control signal based on generated ramp profiles (see Fig. 1, ref. 17).

6. Claims **1-14, 16-27, 38-47** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Lee** (US 2003/0152056) in view of **Lin** (US 2004/0038701) and **Blake** (US 6,847,904).

Regarding claim **1**, **Lee** discloses an RF apparatus formed using an integrated circuit (see Fig. 3B), comprising

- an power amplifier circuitry formed using the integrated circuit (see [0045] regarding "on-chip" limitation which implies an integrated circuit as well) and
- circuitry for generating a power control signal to control the output power of the RF power amplifier (see [0049]).

Although Lee is silent on a ramp profile, it is clear that the power control signal in Lee would obviously be based on a ramp profile as disclosed by Lin (see [0004], 0005]). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the above teaching Lin to Lee for providing a ramp profile as, so that power control based on a ramp profile according to a transmission condition could be selected for controlling amplifier gain, for further improving the performance of the AGC.

As to the newly added limitation regarding a digital interface for providing an interface between the power amplifier circuit and an external controller, it is noted that Lee in view of Lin would teach an external controller for the power amplifier. Here, although Lee as modified fails to disclose a digital interface for the power amplifier circuit, it is noted that using such a digital interface for controlling the gain of an amplifier is known in the art as disclosed by **Blake** (see Fig. 1 and Abstract), Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the above teaching Blake to Lee for providing a digital interface to the

amplifier as well, for minimizing pin count of the amplifier IC package (see Blake, col. 5, lines 55-60).

Regarding claims **2-3,** it is clear that Lee as modified would disclose the digital interface comprises an external controller as claimed (see Blake, Fig. 1 and col. 6, lines 20-24).

Regarding claims **4-6**, since **Lin** discloses a ramp profile for temperature gain control (see [0004]), this would implicitly require a temperature sensor for measurement. Therefore, Lin would disclose one or more sensor and one or more ramp profile based on information from the sensor. Since controlling amplifier based on temperature information is well known in the art, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the above teaching Lin to Lee for providing a temperature sensor and a ramp profile based on temperature information as claimed, for stabilizing the gain control caused by temperature changes.

Regarding claim 7, since Lin also discloses a ramp profile for battery voltage (see [0004]), it would have been obvious to one skilled in the art at the time the invention was made to further incorporate the above teaching Lin to Lee for providing a voltage sensor and a ramp profile based on voltage information as claimed, for stabilizing the gain control caused by voltage level changes.

Regarding claim 8, since using an external control signal for controlling amplifier based on transmission mode (analog mode or digital mode) is known in the art (Official Notice), and since Lin also discloses a plurality of stored ramp profiles for selecting a ramp profile based on transmission conditions such as temperature, voltage of a

battery, and transmission frequency (see [0004]), it would have been obvious to one skilled in the art at the time the invention was made to further modify Lin and Lee for providing an external control signal to control the amplifier based on transmission mode or transmission frequency (i.e, transmission frequency for analog mode and transmission frequency for digital mode are different), and in combination with information from one or more sensors as well, for further improving the performance of the AGC.

Regarding claims 9-10, since Lin also discloses a processor (see Fig. 1 or 3), which may be a DSP (see [0006]) for controlling amplifier gain, it would have been obvious to one skilled in the art at the time the invention was made to further incorporate the above teaching Lin to Lee for providing a DSP to control the amplifier gain as well, so that a plurality of ram profiles could be generated by the DSP for controlling amplifier gain, for further improving the performance of the AGC. By doing so, the DSP in view of Lee would be formed using the integrated circuit.

Regarding claims 11-12, the external control signal is rejected for the same reason as set forth in claim 8 above.

Regarding claim 13, it is clear that Lee in view of Lin would teach a serial interface using the integrated circuit for downloading ramp profiles (see Lin, [0018]) onto the integrated circuit (see Lee, Fig. 3A, [0053]).

Regarding claim 14, it would have been obvious to one skilled in the art that the timing control unit 506 in Fig. 5 of Lee would provide a clock signal for the DSP in order to synchronize operations of the DSP and other I/O interfaces.

Regarding claim 16, Lin discloses a DAC as claimed (see Fig. 1, ref. 114)

Regarding claim 17, it is clear that Lee in view of Lin would teach the RF apparatus comprises memory formed using the integrated circuit, wherein the memory stores a plurality of ramp profiles for controlling the output power of the power amplifier.

Regarding claim 18, Lin discloses a plurality of stored ramp profiles and a selection as claimed (see [0018]).

Regarding claim 19, the received power control signal is interpreted as an external control signal and is rejected the same reason as set forth in claim 8 above.

Regarding claims 20-22, the claims are rejected the same reason as set forth in claims 4-6 above.

Regarding claim 23, the claim is rejected the same reason as set forth in claim 8 above.

Regarding claim 24, the claim is rejected the same reason as set forth in claim 18 above.

Regarding claim 25, Lin discloses a DAC as claimed (see Fig. 1, ref. 114).

Regarding claims 26-27, the DSP is rejected for the same reason as set forth in claims 9-10 above.

Regarding claim 38, the claim is rejected the same reason as set forth in claim 1 above, wherein the "on-chip" amplifier would read on the "first integrated circuit", the "WLAN transceiving integrated circuit" for controlling amplifier power would read on the "second integrated circuit" (see [045], [0049]).

Regarding claims 39-40, the claims are rejected the same reason as set forth in claim 38 above. In addition, since the use of either GaAs substrate or silicon substrate for amplifiers is well known in the art, it would have been obvious to one skilled in the art at the time the invention was made to further modify Lee for providing substrates as claimed, for utilizing advantages of each substrate such as cost and/or performance quality.

Regarding claim 41, the claim is rejected the same reason as set forth in claim 38 above. In addition, it would have been obvious to use a printed circuit board as claimed, for utilizing advantages of the printed circuit board such as easy interface connection.

Regarding claim 42, the claim is rejected the same reason as set forth in claim 38 above. In addition, it would have been obvious to use a substrate as claimed, for utilizing advantages of the substrate such as low power dissipation.

As to claims 43-47, Lin would disclose sensors, DSP, ram profiles and DAC for the same reason as set forth in claims 4-8, 16 above (see also Fig. 1 and [0018]).

7. Claims **15, 28** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Lee** in view of **Lin** and **Blake**, and further in view of **Yu et al** (US 5,365,190).

As to claims 15, 28, the claims are rejected the same reason as set forth in claim 14 above. However, Lee fails to disclose the clock signal is generated by dividing the RF input signal. However, Yu discloses an RF device wherein the clock signal is generated by dividing the RF input signal. Therefore, it would have been obvious to one

skilled in the art at the time the invention was made to provide Yu's teaching to Lee, to generate the clock signal by dividing the RF input signal as well, for cost saving.

8. Claims **29-37** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Lee** in view of **Lin** and **Blake**, and further in view of **Gunzelmann et al** (US 2004/0097250).

As to claim 29, the claim is rejected the same reason as set forth in claim 18 above. In addition, since Lee discloses a baseband section (see Fig. 4A), Lin discloses a DSP for controlling amplifier power, and since utilizing a DSP at a baseband controller to control power of the amplifier is known in the art as disclosed by Gunzelmann (see Fig. 1 and [0043], [0068]), it would have been obvious to one skilled in the art at the time the invention was made to use Gunzelmann's teaching to integrate the DSP in Lin at the baseband section in Lee as well, so that the digital characteristics of the DSP circuit and the baseband section circuit can be efficiently formed in a singe integrated circuit, for cost and size reduction.

As to claims 30-31, Gunzelmann discloses the digital interface comprises serial interfaces as claimed (see [0061]-[0063]).

As to claims 32-37, Lin would disclose sensors, DSP, ram profiles and DAC for the same reason as set forth in claims 4-8, 16 above (see also Fig. 1 and [0018]).

Conclusion

9. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(571) 273-8300 (for **formal** communications intended for entry)

(571)-273-7893 (for informal or **draft** communications).

Hand-delivered responses should be brought to Customer Service Window, Randolph Building, 401 Dulany Street, Alexandria, VA 22314.

Any inquiry concerning this communication or communications from the examiner should be directed to Duc M. Nguyen whose telephone number is (571) 272-7893, Monday-Thursday (9:00 AM - 5:00 PM).

Or to Matthew Anderson (Supervisor) whose telephone number is (571) 272-4177.

Duc M. Nguyen, P.E.

July 28, 2007